CCB021M12FM3

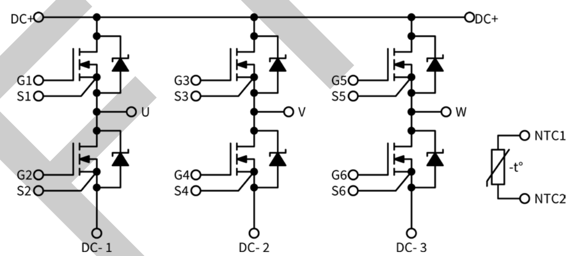
1200 V, 21 mΩ All-Silicon Carbide Six-Pack Module

V_{DS}	1200 V
$R_{DS(on)}$	21 mΩ

Technical Features

- Ultra-Low Loss
- High Frequency Operation
- Zero Turn-Off Tail Current from MOSFET
- Normally-Off, Fail-Safe Device Operation

Package



Applications

- EV Chargers
- Solar
- High-Efficiency Converters / Inverters
- Motor & Traction Drives
- Smart-Grid / Grid-Tied Distributed Generation

System Benefits

- Enables Compact, Lightweight Systems
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

Maximum Parameters (Verified by Design)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{DS\ max}$	Drain-Source Voltage			1200	V		
$V_{GS\ max}$	Gate-Source Voltage, Maximum Value	-8		+19	V	Transient, <100 ns	Fig. 32
$V_{GS\ op}$	Gate-Source Voltage, Recommended Op. Value	-4		+15	V	Static	Fig. 32
I_{DS}	DC Continuous Drain Current		30		A	V_{GS} = 15 V, T_H = 50 ˚C, T_{VJ} ≤ 175 ˚C Limited by the pins.	Fig. 20
I_{SD}	DC Source-Drain Current		30		A	V_{GS} = 15 V, T_H = 50 ˚C, T_{VJ} ≤ 175 ˚C Limited by the pins.	Fig. 20
$I_{SD\ BD}$	DC Source-Drain Current (Body Diode)				A	V_{GS} = - 4 V, T_H = 50 ˚C, T_{VJ} ≤ 175 ˚C	
$I_{DS\ (pulsed)}$	Maximum Pulsed Drain-Source Current				A	t_{Pmax} limited by T_{jmax} V_{GS} = 15 V, T_H = 50 ˚C	
$I_{SD\ (pulsed)}$	Maximum Pulsed Source-Drain Current				A	t_{Pmax} limited by T_{jmax} V_{GS} = 15 V, T_H = 50 ˚C	
$T_{VJ\ op}$	Maximum Virtual Junction Temperature under Switching Conditions	-40		150	°C	Operation	
		-40		175	°C	Intermittent with Reduced Life	

MOSFET Characteristics (Per Position) (T_{VJ} = 25 ˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
$V_{GS(th)}$	Gate Threshold Voltage					V_{DS} = V_{GS}, I_D = xx mA	
I_{DSS}	Zero Gate Voltage Drain Current				µA	V_{GS} = 0 V, V_{DS} = 1200 V	
I_{GSS}	Gate-Source Leakage Current					V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance (Devices Only)		21		mΩ	V_{GS} = 15 V, I_D = 30 A	Fig. 2 Fig. 3
			32.6			V_{GS} = 15 V, I_D = 30 A, T_{VJ} = 150 °C	
			38			V_{GS} = 15 V, I_D = 30 A, T_{VJ} = 175 °C	
g_{fs}	Transconductance				S	V_{DS}= 20 V, I_{DS}= 30 A	Fig. 4
						V_{DS}= 20 V, I_{DS}= 30 A, T_{VJ} = 175 °C	
E_{On}	Turn-On Switching Energy, T_J = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C				mJ	V_{DS} = 600 V, I_D = 30 A, V_{GS} = -4 V/15 V, $R_{G(OFF)}$ = x.0 Ω, $R_{G(ON)}$ = x.0 Ω L= xx.x µH	Fig. 11 Fig. 13
E_{Off}	Turn-Off Switching Energy, T_J = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C						
$R_{G(int)}$	Internal Gate Resistance		3.3		Ω	T_{VJ} = 25 °C, f = 100 kHz, V_{AC} = 25 mV	
C_{iss}	Input Capacitance				nF	V_{GS} = 0 V, V_{DS} = 1000 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
C_{oss}	Output Capacitance						
C_{rss}	Reverse Transfer Capacitance				pF		
Q_{GS}	Gate to Source Charge				nC	V_{DS} = 600 V, V_{GS} = -4 V/15 V I_D = 30 A Per IEC60747-8-4 pg 21	
Q_{GD}	Gate to Drain Charge						
Q_G	Total Gate Charge						
$R_{th\ JH}$	FET Thermal Resistance, Junction to Heatsink		1.16		°C/W		Fig. 17

CREE Wolfspeed

Diode Characteristics (Per Position) (T_{VJ} = 25 ˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Body Diode Forward Voltage				V	V_{GS} = -4 V, I_{SD} = 30 A	Fig. 7
						V_{GS} = -4 V, I_{SD} = 30 A, T_{VJ} = 175 °C	
t_{rr}	Reverse Recovery Time				ns	V_{GS} = -4 V, I_{SD} = 30 A, V_R = 600 V di/dt = xx.x A/ns, T_J = 150 °C	Fig. 31
Q_{RR}	Reverse Recovery Charge				µC		
I_{RRM}	Peak Reverse Recovery Current				A		
E_{RR}	Reverse Recovery Energy T_J = 25 °C T_J = 125 °C T_J = 150 °C				mJ	V_{DS} = 600 V, I_D = 30 A, V_{GS} = -4 V/15 V, $R_{G(ON)}$ = x.0 Ω, L= x.x µH	Fig. 14

Module Physical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
R_{1-2}	Package Resistance, M1		TBD		µΩ	T_C = 125 °C, Note 2
R_{2-3}	Package Resistance, M2		TBD			T_C = 125 °C, Note 2
L_{Stray}	Stray Inductance		TBD		nH	Between Terminals DC+ and DC-
T_C	Case Temperature	-40		125	°C	
W	Weight		TBD		g	
M_S	Mounting Torque		2.0	2.3	N-m	M4 bolts
V_{isol}	Case Isolation Voltage		3		kV	AC, 50 Hz, 1 min
CTI	Comparative Tracking Index	200				
	Clearance Distance		TBD		mm	Terminal to Terminal
			TBD			Terminal to Heatsink
	Creepage Distance		TBD			Terminal to Terminal
			TBD			Terminal to Heatsink

Note 2 Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance.

Typical Performance

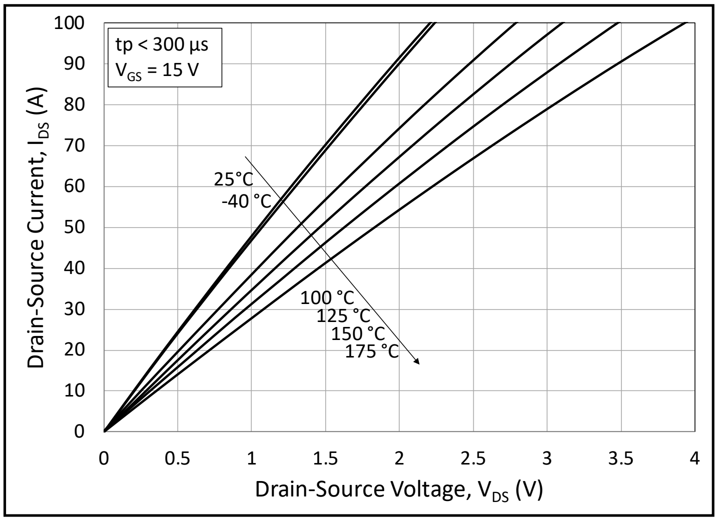


Figure 1. Output Characteristics for Various Junction Temperatures

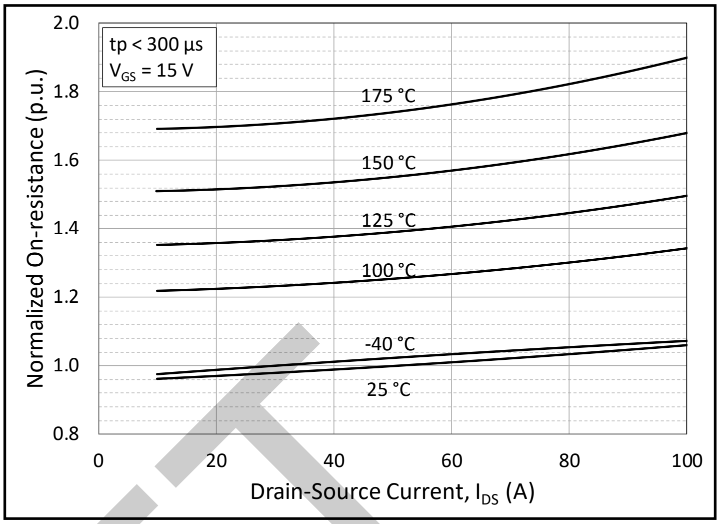


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Juction Temperatures

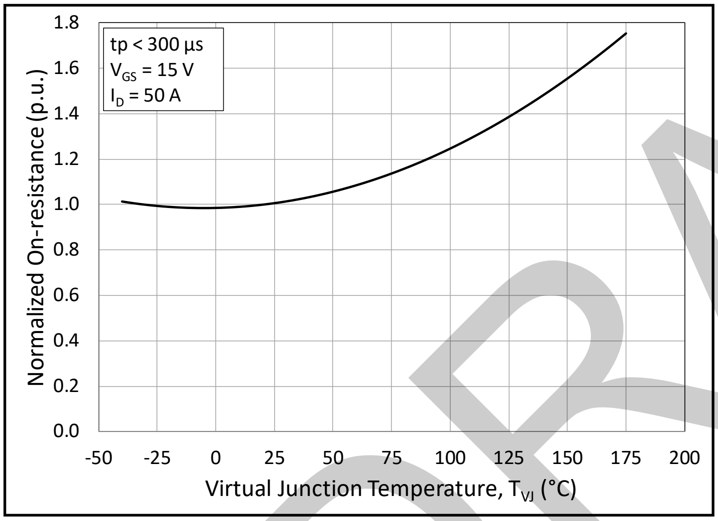


Figure 3. Normalized On-State Resistance vs. Juction Temperature

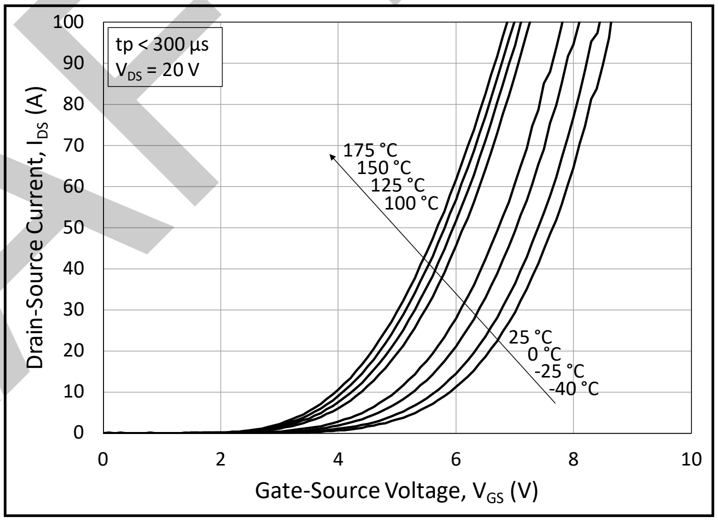


Figure 4. Transfer Characteristic for Various Junction Temperatures

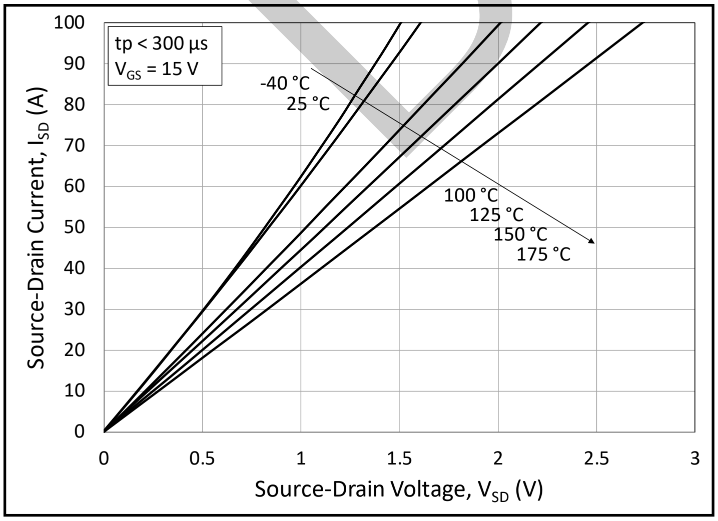


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

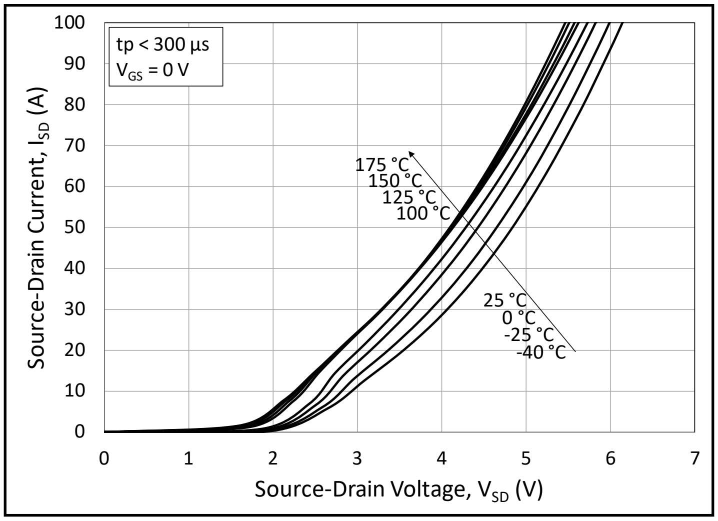


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Body Diode)

Typical Performance

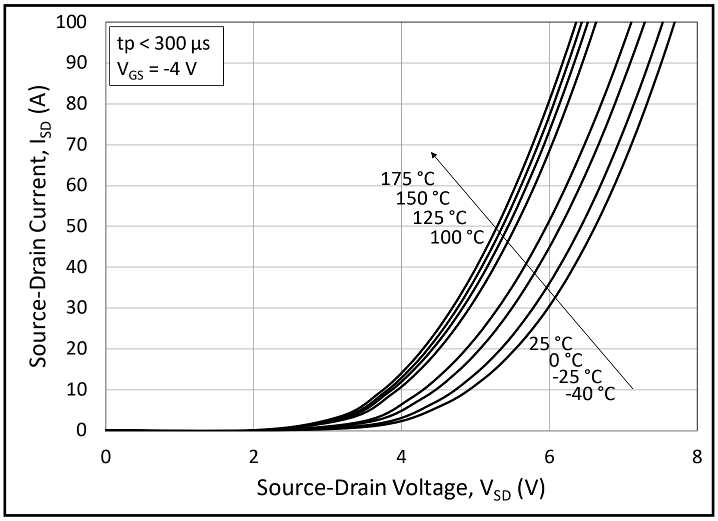


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = - 4 V (Body Diode)

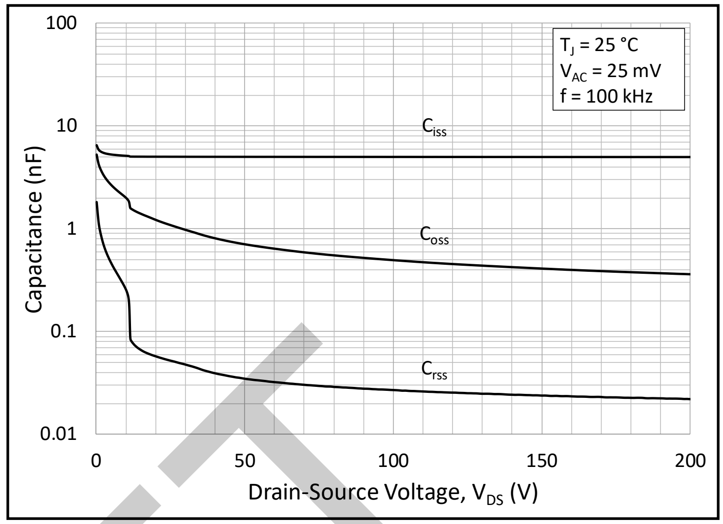


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

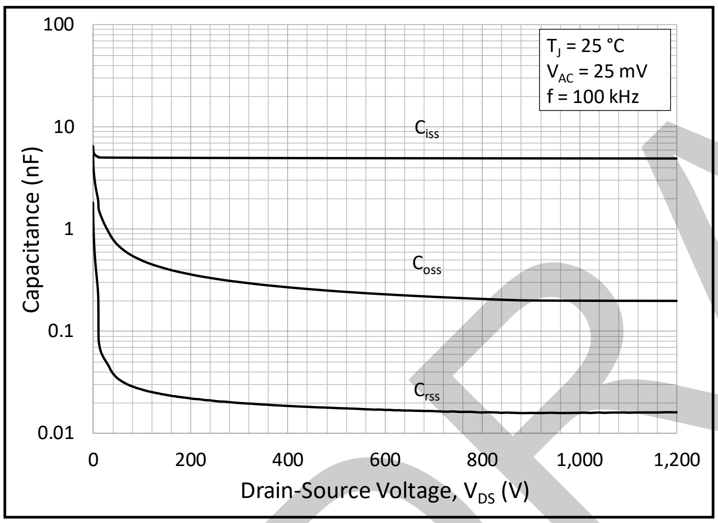


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

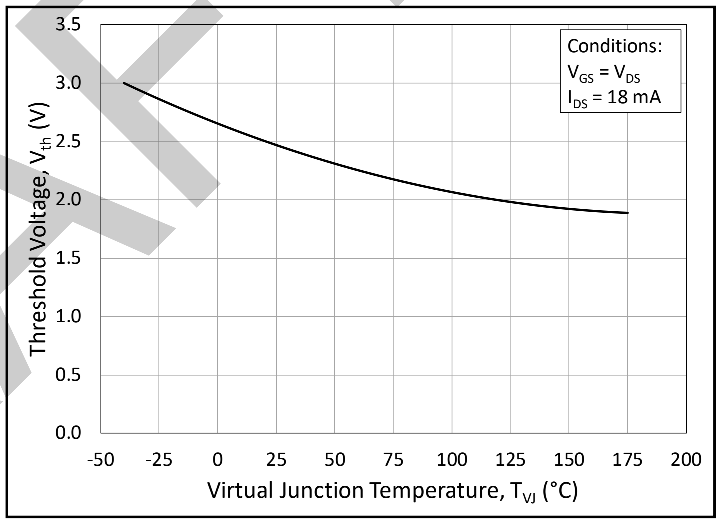


Figure 10. Threshold Voltage vs. Junction Temperature

Figure 11. Switching Energy vs. Drain Current (V_{DS} = 600 V)

Figure 12. Switching Energy vs. Drain Current (V_{DS} = 800 V)

Typical Performance

Figure 13. MOSFET Switching Energy vs. Junction Temperature

Figure 14. Reverse Recovery Energy vs. Junction Temperature

Figure 15. MOSFET Switching Energy vs. External Gate Resistance

Figure 16. Reserve Recovery Energy vs. External Gate Resistance

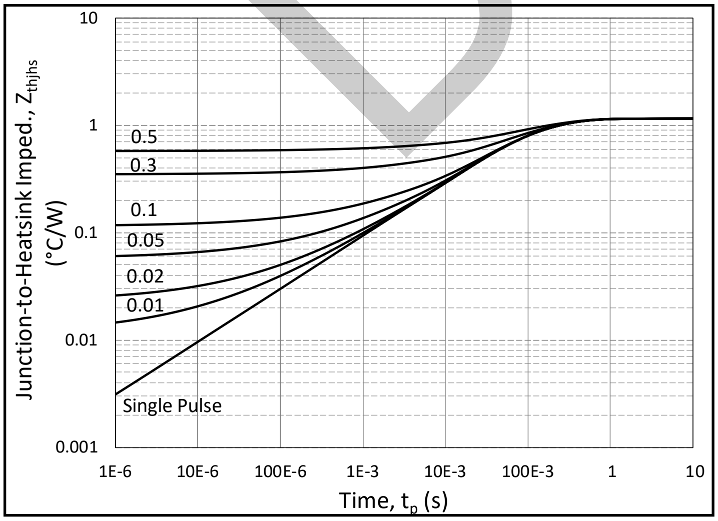


Figure 17. MOSFET Juction to Case Transient Thermal Impedance, $Z_{th\ JC}$ (°C/W)

Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

Figure 19. Reverse Bias Safe Operating Area (RBSOA)

Figure 20. Continuous Drain Current Derating vs. Case Temperature

Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

Figure 22. Typical Ouput Current Capablity vs. Switching Frequency (Inverter Application)

Timing Characteristics

Figure 23. Timing vs. Source Current

Figure 24. Timing vs. External Gate Resistance

Figure 25. Timing vs. Junction Temperature

Figure 26. dv/dt and di/dt vs. Source Current

Figure 27. dv/dt and di/dt vs. External Gate Resistance

Figure 28. dv/dt and di/dt vs. Junction Temperature

Definitions

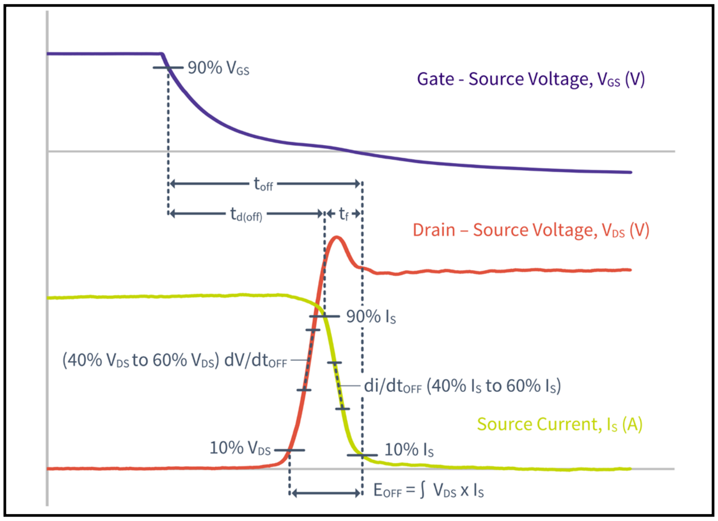


Figure 29. Turn-off Transient Definitions

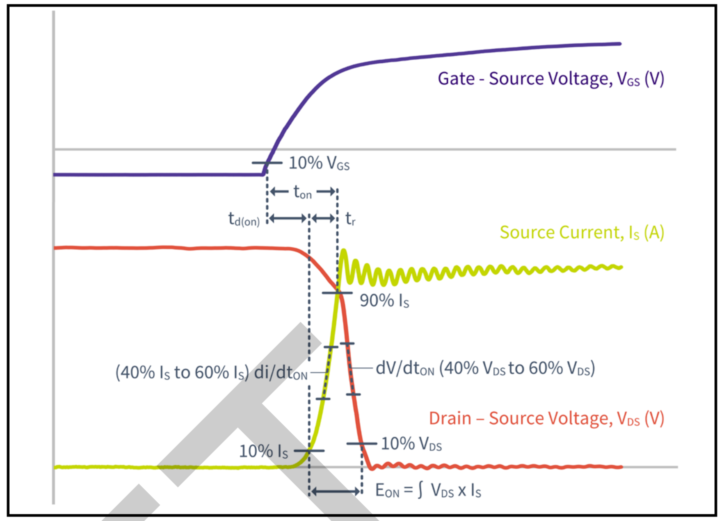


Figure 30. Turn-on Transient Definitions

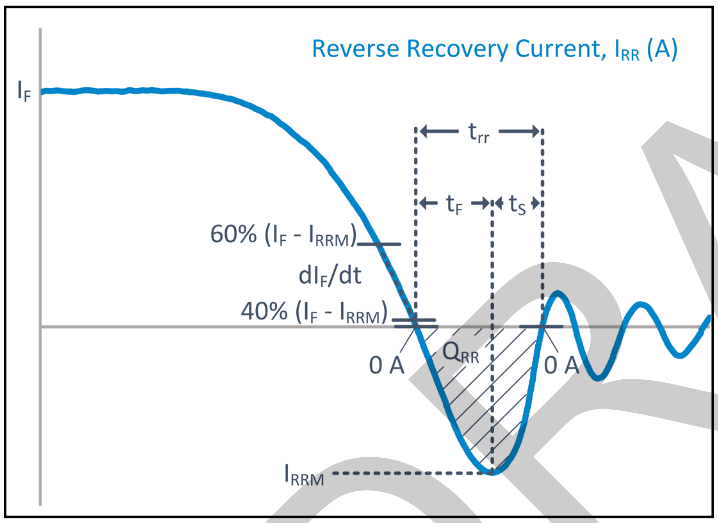


Figure 31. Reverse Recovery Definitions

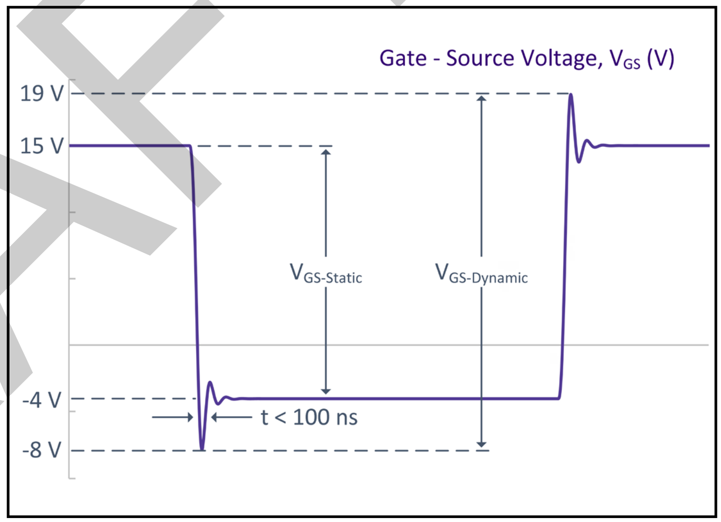
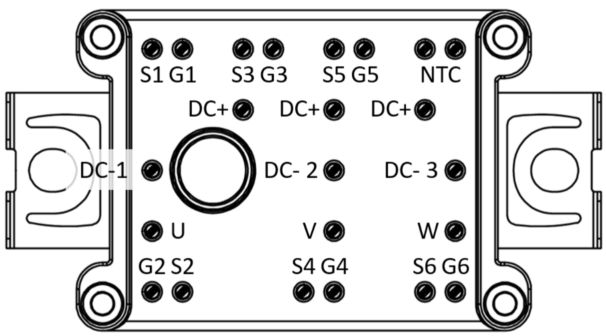
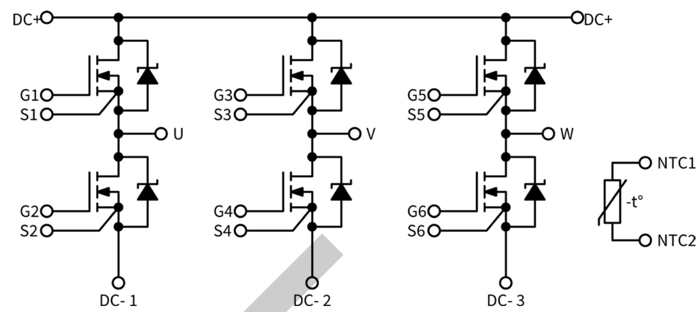


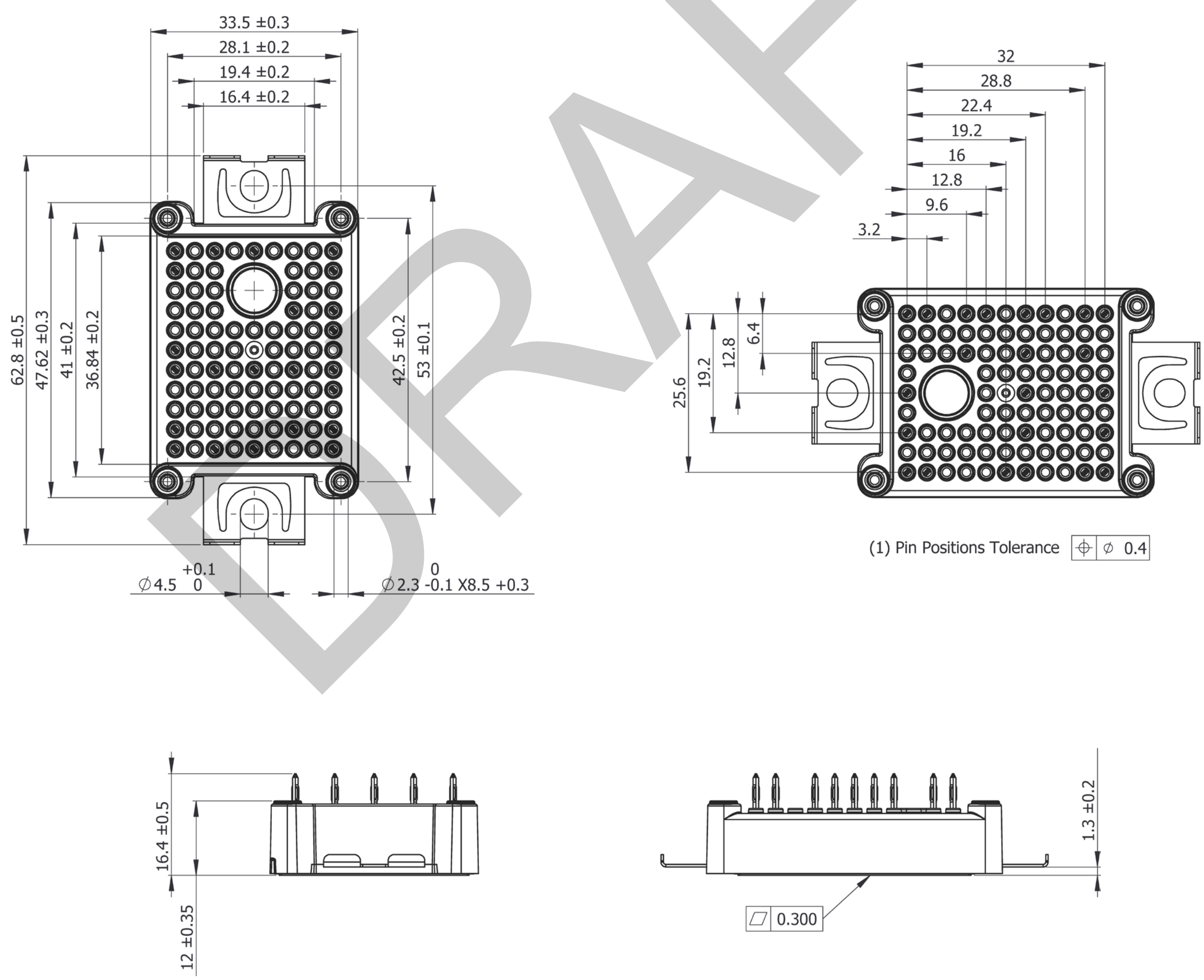
Figure 32. V_{GS} Transient Definitions

Schematic and Pin Out





Package Dimension (mm)



Supporting Links & Tools

- WolfPACK SiC Power Modules Family
- Companion Gate Driver Boards
- KIT-CRD-CIL12N-FMA: Dynamic Evaluation Board for Half-Bridge FM3 Modules
- KIT-CRD-CIL12N-FMC: Dynamic Evaluation Board for Six-Pack FM3 Modules

Notes

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.

- The SiC MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.