Test Report :

Driving Wolfspeed® C3M™ 650V 7-pin D2PAK SiC MOSFETs with Analog Devices® ADuM4121 in Synchronous Boost applications

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1. Introduction

The purpose of the test report is to document the results of testing performed to characterize the switching characteristics (double pulse), efficiency and thermal performance of Wolfspeed C3M™ 650V 7-pin D2PAK MOSFETs (C3M0060065J) when driven in a synchronous boost configuration with an Analog Devices® ADuM4121 gate driver.

This document along with the user guide for Evaluation kit KIT-CRD-8FF65P may be used to assess the feasibility of new designs using Wolfspeed C3M™ 650V 7-pin D2PAK MOSFETs with ADuM4121 gate drivers.

2. Background

Non-isolated DC-DC synchronous buck and synchronous boost converters are a popular choice for energy storage systems, industrial power supply and DC-DC converters for electric vehicles. Synchronous boost topologies eliminate the diode loss seen in asynchronous variants, especially at high output currents. SiC MOSFETs offers the benefits of a low diode Q_{rr}, reduced switching losses, low C_{oss} and low $R_{ds(on)}$ which can increase the efficiency of the converters. The use of 7-pin D2PAK packages further reduces parasitic inductances and improve thermal spreading, enabling higher power designs. The ADuM4121 gate driver's low Rds(on) (<2 Ω) provides enough gate drive current to allow the MOSFETs to be driven as fast as 55kV/µs in this test setup. The high common mode transient immunity (CMTI) of >150KV/µs supports data integrity during these fast transitions while an internal Miller clamp prevents any Miller capacitance induced turn on.

3. Test Setup

This section describes the set up for Cree's KIT-CRD-8FF65P Evaluation Kit in a Synchronous Boost Converter topology (Fig. 1 and Table 1). The electrical parameters for the test setup are shown below in Figure 1 and Figure 2. The KIT-CRD-8FF65P has been modified thermally for this experiment to enable higher power testing but the electrical circuits were unchanged.

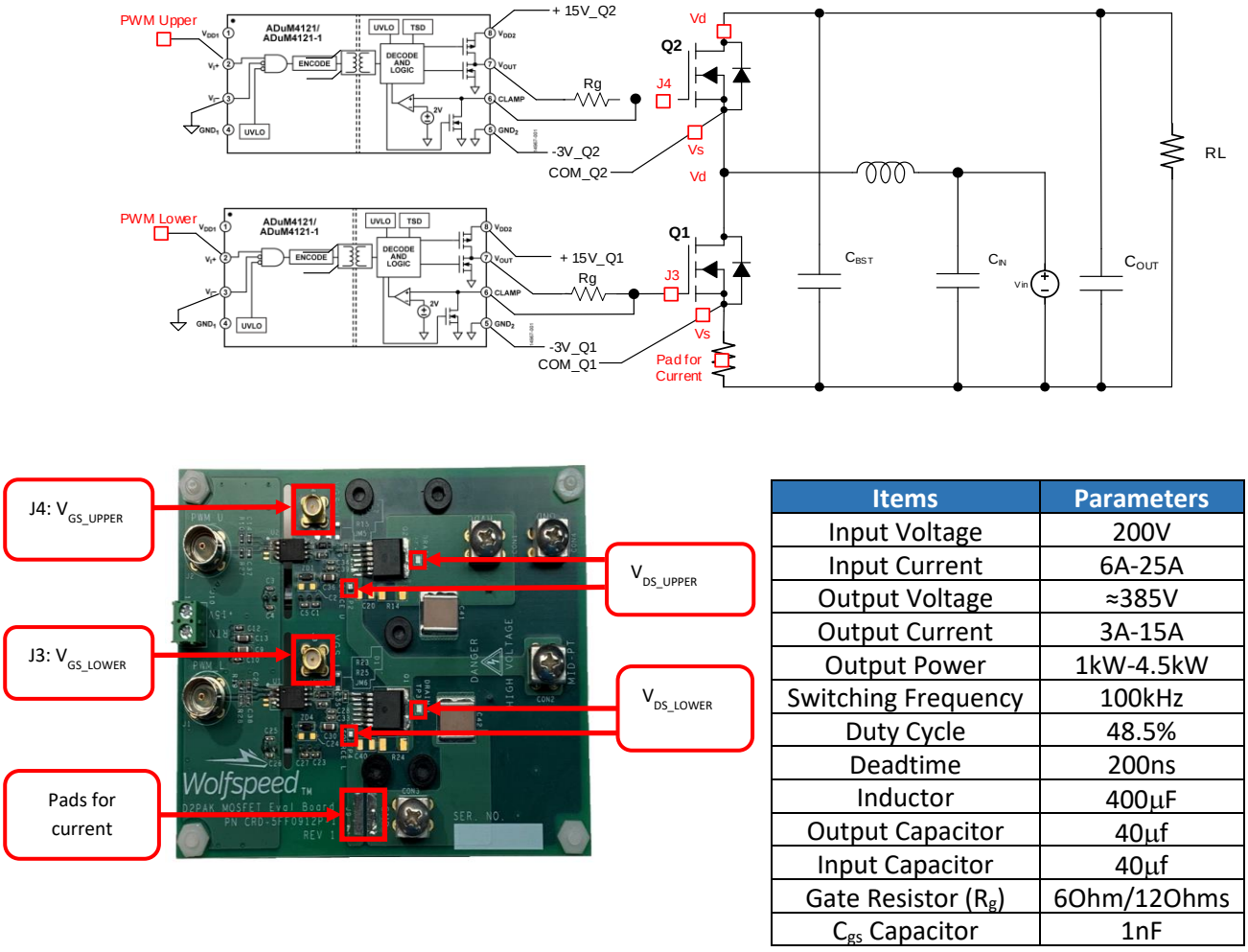

Figure 1. Test setup and parameters

Items	Parameters
Input Voltage	200V
Input Current	6A-25A
Output Voltage	≈385V
Output Current	3A-15A
Output Power	1kW-4.5kW
Switching Frequency	100kHz
Duty Cycle	48.5%
Deadtime	200ns
Inductor	400µF
Output Capacitor	40µf
Input Capacitor	40µf
Gate Resistor (R_g)	6Ohm/12Ohms
C_{gs} Capacitor	1nF

Table 1. Test setup parameters

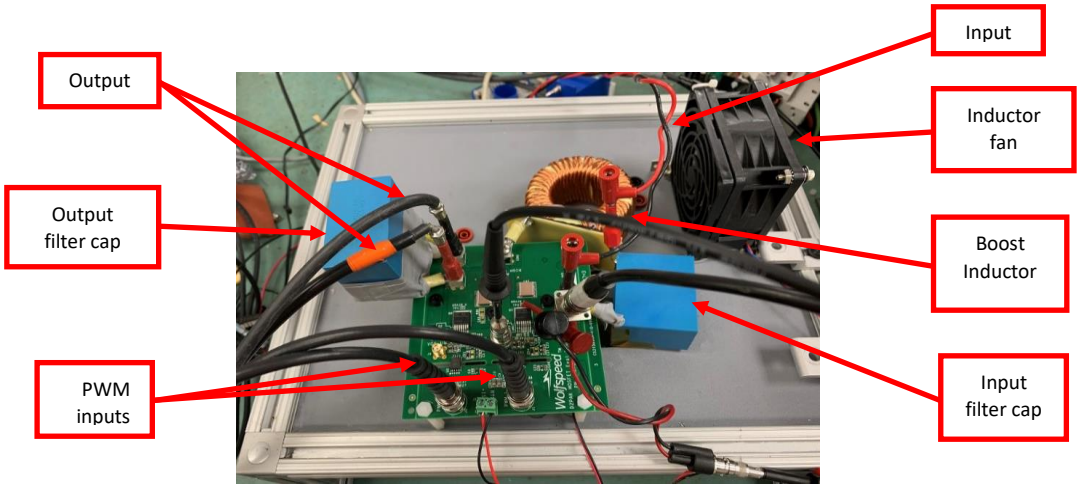

Figure 2. Board Setup

3.1 Test Procedure

An SMA to BNC adapter should be connected to J3 (V_{GS} lower MOSFET). A 10X compensated passive oscilloscope probe with a BNC connector is then attached with J3 to monitor the V_{GS} on the lower MOSFET (Fig. 18). A 10mΩ current viewing resistor from T&M Research (P/N: SDN-414-01) is populated at J9 to get current measurements through the lower MOSFET. Since the lower MOSFET is referenced to the -DC link along with the V_{GS} probe, a 100X high voltage passive probe is attached to the drain and power source of the lower MOSFET to capture V_{DS}. The current shunt is actually installed backwards so that its common is connected to the same node as V_{DS} and V_{GS} (all three probes are referenced to the same point or the MOSFET source).

The bridge was operated with a fixed duty-cycle and the operating points were obtained by varying R_{load}. The measurements for efficiency, switching energy and temperature were taken at two different values of the gate resistor R_g.

Efficiency measurements

Efficiency measurements are taken with Yokogawa® WT1600 digital power meter.

Voltages are taken directly from the input and output terminals of the CRD8FF6590P evaluation board. Input and output currents are measured using LEM current sensor

(IT 200-S Ultrastab) and IST ULTRASTAB power supply.

Figure 3. Equipment used for efficiency measurements

Switching energy measurements

The switching energy measurements are taken by multiplying V_{DS} and I_{DS} during the turn-on and turn-off event. The product of V_{DS} and I_{DS} yields the switching power waveform (purple). To get the energy, you simply take the area underneath the power curve (purple) during turn-off or turn-on. The two channels being multiplied must be de-skewed to yield accurate measurements.

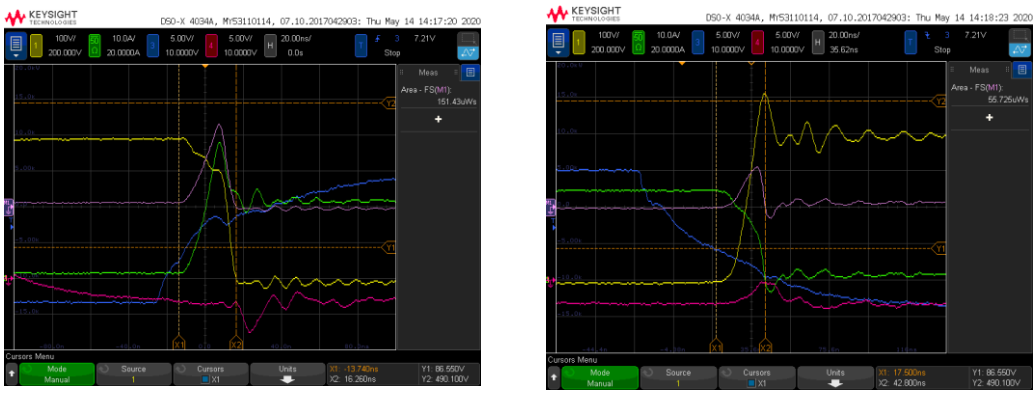

Figure 4. Examples of Turn On (L) and Turn Off (R) signals used for efficiency calculations

Thermal Measurements

All thermal measurements are taken with a FLIR® T420 IR camera like the one shown below

Figure 5. Thermal camera used for measurements

4. Test Results

4.1 Summary of Results

The test results for efficiency, switching energy and MOSFET temperature are summarized for the two values of the gate resistor, R_g.

Efficiency Measurements

Rg	Test Case	Input Voltage	Input Current	Input Power	Output Voltage	Output Current	Output Power	Overall Efficiency
Ohms		(Vdc)	(A)	(W)	(Vdc)	(A)	(W)	(%)
6	1kW	199.46	6.2	1236.8	386.61	3.1657	1224.1	98.97
	2kW	199.35	9.227	1839.9	385.34	4.724	1820.8	98.96
	2.5kW	199.26	12.284	2448.1	384.32	6.296	2420	98.85
	3kW	199.17	15.301	3048	383.68	7.839	3008.2	98.69
	3.5kW	199.06	18.297	3643	382.61	9.373	3587	98.45
	4kW	198.96	21.294	4237	381.43	10.909	4162	98.22
	4.5kW	198.47	24.235	4811	379.3	12.415	4710	97.90
12	1kW	200.75	6.259	1256.7	390.06	3.1836	1242	98.83
	2kW	200.66	9.309	1868.3	388.88	4.747	1846.6	98.84
	2.5kW	200.55	12.41	2489.2	387.76	6.336	2457.4	98.72
	3kW	200.42	15.433	3093.6	386.67	7.883	3048.7	98.55
	3.5kW	200.35	18.445	3696	385.24	9.429	3633	98.29
	4kW	199.15	21.407	4264	382.25	10.935	4181	98.04

Table 2. Measured Efficiency

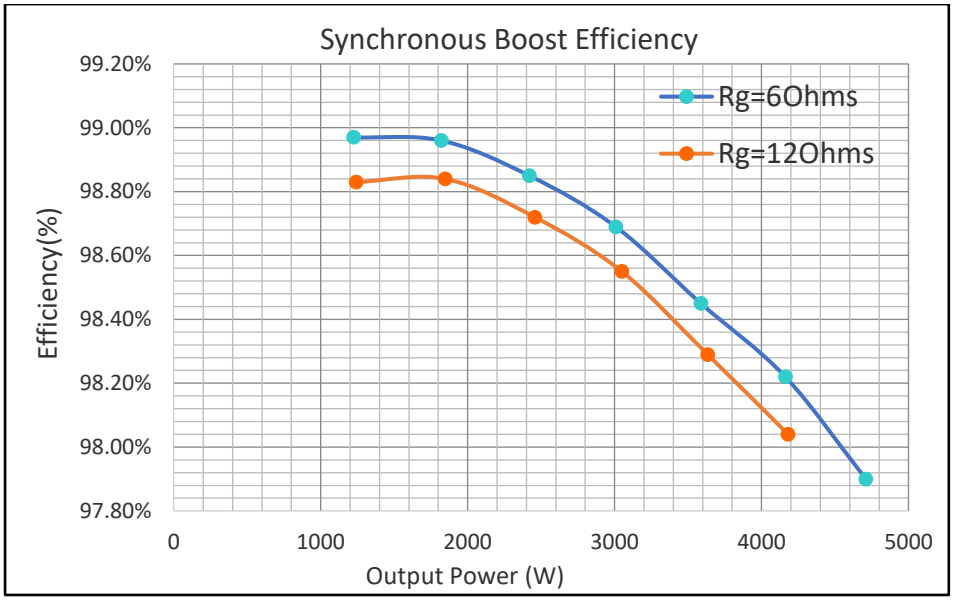

Figure 6. Measured Efficiency

Switching energy and dv/dt measurements

Rg	Test Case	dv/dt (turn-on)	dv/dt (turn-off)	Eon	Eoff
Ohms		V/ns	V/ns	µJ	µJ
6	3.5kW	54.9	49.8	100.4	20
	4kW	51.6	51.8	114.8	27.2
	4.5kW	47.7	52.9	129.6	34.8
12	3.5kW	42.2	33.4	130.7	44.8
	4kW	43.7	34.5	151.4	55.7

Table 3. Measured dv/dt and switching energy

Temperature Measurements

Rg	Test Case	Output Power	Ambient Temp	Lower MOSFET Q1 Case Temp	Upper MOSFET Q2 Case Temp	Upper Gate Driver GD1 Case Temp	Lower Gate Driver GD2 Case Temp
Ohms		(W)	(C)	(C)	(C)	(C)	(C)
6	1kW	1224.1	23	34.4	31.6	-	-
	2kW	1820.8	23.1	39.7	36.5	-	-
	2.5kW	2420	24	50.3	46.7	-	-
	3kW	3008.2	24	62.4	58.5	-	-
	3.5kW	3587	24	76.2	72	-	-
	4kW	4162	24.4	94.8	89	-	-
	4.5kW	4710	25.2	120	111.2	-	-
12	1kW	1242	22.7	37.8	33	30.6	28.5
	2kW	1846.6	23.3	46.4	40.3	-	-
	2.5kW	2457.4	23.7	57.3	48.9	-	-
	3kW	3048.7	24.3	72.2	62.2	-	-
	3.5kW	3633	25	89.6	77.1	37.5	32.7
	4kW	4181	25.6	112.8	96		

Table 4. Measured dv/dt, switching energy and temperature measurements

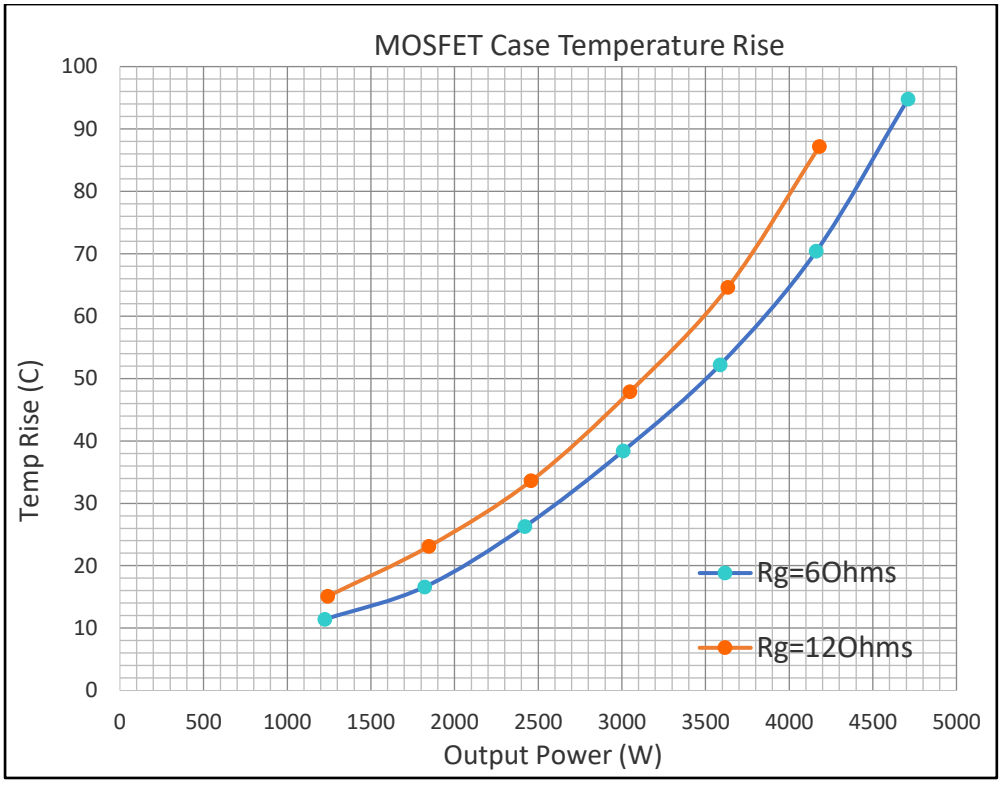

Figure 7. MOSFET Q1 temperature rise

5. Observations

High efficiencies of close to 99% along with well managed MOSFET and gate driver temperature rise can be achieved even at power levels of 4.5kW. High switching slew rates of 55kV/μs have been demonstrated for high efficiencies without disturbances in the gate driver propagation delay or the possibility of Miller induced turn-on. The internal Miller clamp on the AduM4121 provides the driven gate with a lower impedance path to reduce the chance of Miller capacitance induced turn on.

6. Test Data

Oscilloscope plots of relevant signals are summarized in this section. The key for the plots is consistent for all plots in this set :

Green = MOSFET Q1 IDS

Blue = MOSFET Q1 Vgs

Pink = MOSFET Q2 Vgs (diff probe)

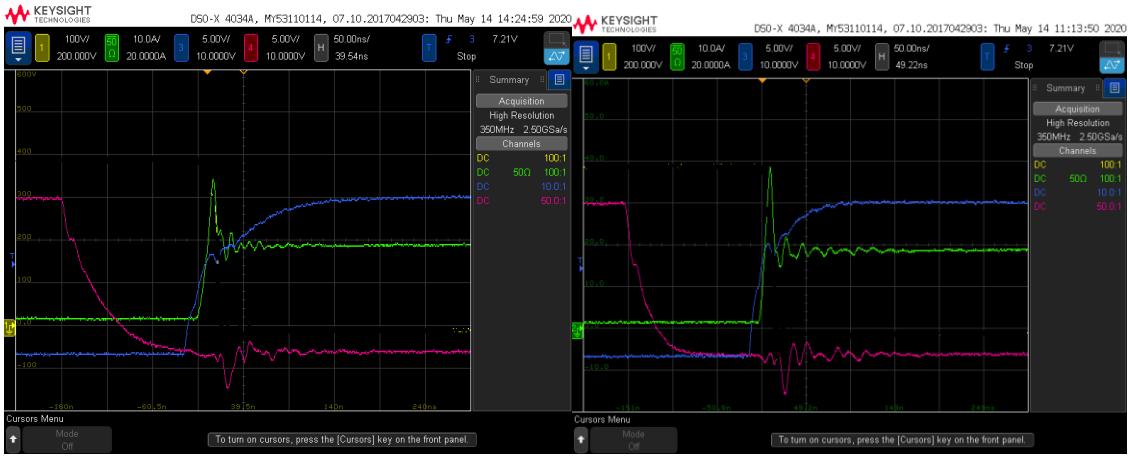

Figure 8 : Switching transition (1) at 3.5kW for Rg=12 (left) and Rg=6 (right). Note that the negative voltage seen on the Q2 Vgs is a measurement artifact

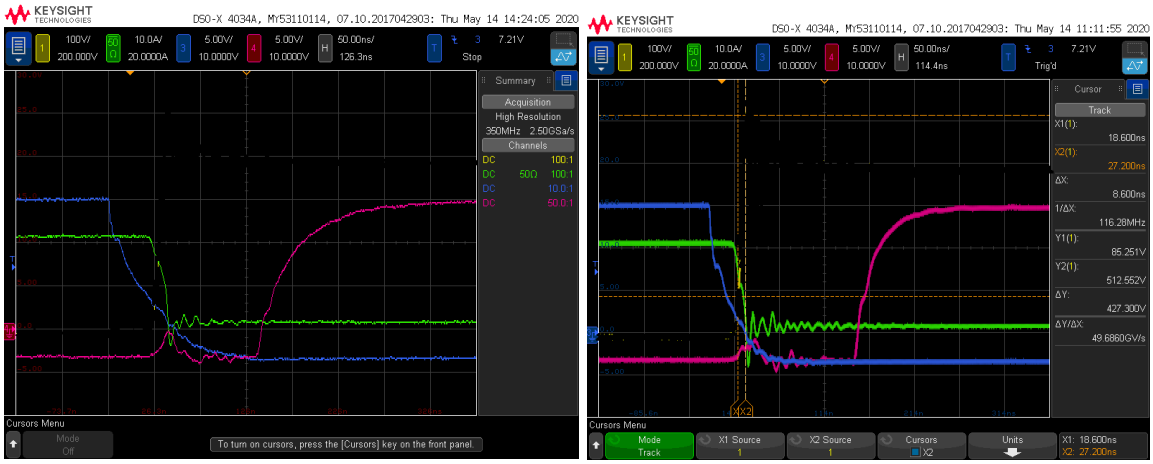

Figure 9 : Switching transition (2) at 3.5kW for Rg=12 (left) and Rg=6 (right)