GAN039-650NBBA

650 V, 33 mOhm Gallium Nitride (GaN) FET in a CCPAK1212 package

19 April 2021 **Objective data sheet**

1. General description

The GAN039-650NBBA is an Automotive qualified 650 V, 33 mΩ Gallium Nitride (GaN) FET in a CCPAK1212 package. It is a normally-off device that combines Nexperia's latest high-voltage GaN HEMT H2 technology and low-voltage silicon MOSFET technologies — offering superior reliability and performance.

This product has been fully designed and qualified to meet AEC-Q101 requirements.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Simplified driver design as standard level MOSFET gate drivers can be used:
  - 0 V to 12 V drive voltage
  - Gate threshold voltage V_{GSth} of 4 V
- Robust gate oxide with ±20 V V_{GS} rating
- High gate threshold voltage of 4 V for gate bounce immunity
- Low body diode V_f for reduced losses and simplified dead-time adjustments
- Transient over-voltage capability for increased robustness
- CCPAK package technology:
  - Improved reliability, with reduced $R_{th(j-mb)}$ for optimal cooling
  - Lower inductances for lower switching losses and EMI
  - 175 °C maximum junction temperature
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joints

3. Applications

- Automotive On-Board-Charger systems
- Automotive DC-DC
- Hard and soft switching converters for industrial and datacom power
- Bridgeless totempole PFC
- PV and UPS inverters
- Servo motor drives

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 175 °C		-	-	650	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	-	60	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	300	W

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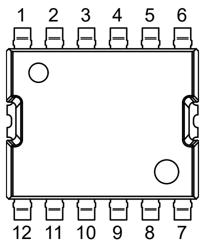
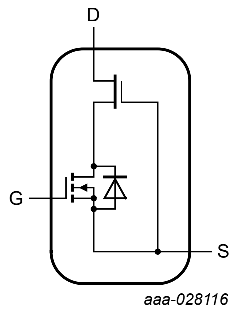
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 32 A; T_j = 25 °C		-	33	39	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 32 A; V_{DS} = 400 V; V_{GS} = 10 V; T_j = 25 °C		-	5	-	nC
$Q_{G(tot)}$	total gate charge			-	30	-	nC
Source-drain diode							
Q_r	recovered charge	I_S = 32 A; dI_S/dt = -1000 A/µs; V_{GS} = 0 V; V_{DS} = 400 V; Fig. 3		-	150	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 CCPAK (SOT8000)	
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	S	source		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	S	mounting base; connected to source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GAN039-650NBBA	CCPAK	Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body	SOT8000

7. Marking

Table 4. Marking codes

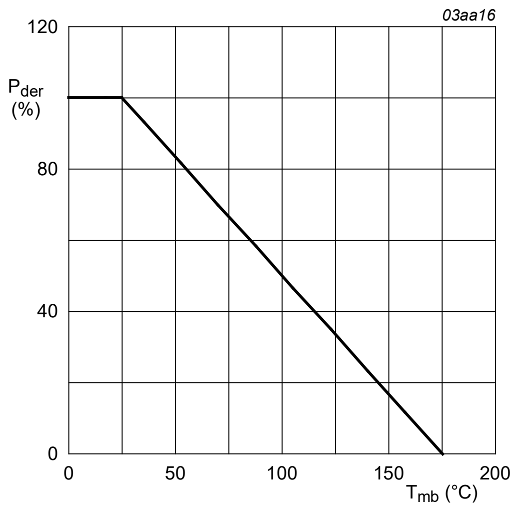
Type number	Marking code
GAN039-650NBBA	039INBBA

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 175 °C		-	650	V
V_{TDS}	transient drain to source voltage	pulsed; t_p = 1 µs; $δ_{factor}$ = 0.01		-	[tbd]	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	300	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	60	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	42	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	240	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C; V_{GS} = 0 V		-	55	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	240	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature

9. Thermal characteristics

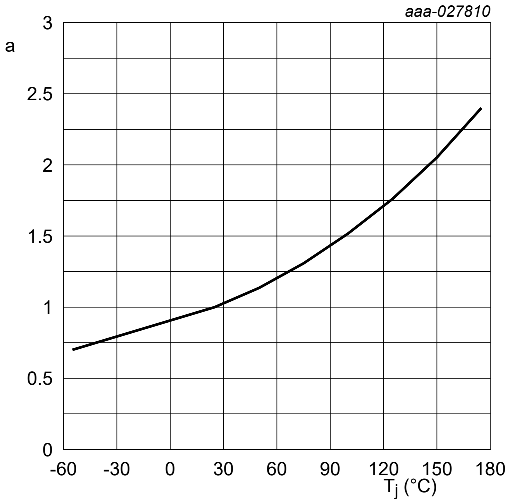
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	-	0.5	K/W

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		3.3	4	4.8	V
I_{DSS}	drain leakage current	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C		-	[tbd]	[tbd]	µA
		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 175 °C		-	[tbd]	-	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	400	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	400	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 32 A; T_j = 25 °C		-	33	39	mΩ
		V_{GS} = 10 V; I_D = 32 A; T_j = 175 °C; Fig. 2		-	80	-	mΩ
R_G	gate resistance	f = 1 MHz		-	1.88	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 32 A; V_{DS} = 400 V; V_{GS} = 10 V; T_j = 25 °C		-	30	-	nC
Q_{GS}	gate-source charge			-	9	-	nC
Q_{GD}	gate-drain charge			-	5	-	nC
C_{iss}	input capacitance	V_{DS} = 400 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		-	1500	-	pF
C_{oss}	output capacitance			-	147	-	pF
C_{rss}	reverse transfer capacitance			-	5	-	pF
$C_{o(er)}$	effective output capacitance, energy related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		-	220	-	pF
$C_{o(tr)}$	effective output capacitance, time related			-	380	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 400 V; R_L = 12.5 Ω; V_{GS} = 12 V; $R_{G(ext)}$ = 30 Ω		-	[tbd]	-	ns
t_r	rise time			-	[tbd]	-	ns
$t_{d(off)}$	turn-off delay time			-	[tbd]	-	ns
t_f	fall time			-	[tbd]	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 400 V		-	150	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 32 A; V_{GS} = 0 V; T_j = 25 °C		-	1.8	-	V
		I_S = 16 A; V_{GS} = 0 V; T_j = 25 °C		-	1.3	-	V
t_{rr}	reverse recovery time	I_S = 32 A; dI_S/dt = -1000 A/µs; V_{GS} = 0 V; V_{DS} = 400 V; Fig. 3		-	[tbd]	-	ns
Q_r	recovered charge			-	150	-	nC



$$a = \frac{R_{DSon}}{R_{DSon}(25°C)}$$

Fig. 2. Normalized drain-source on-state resistance factor as a function of junction temperature

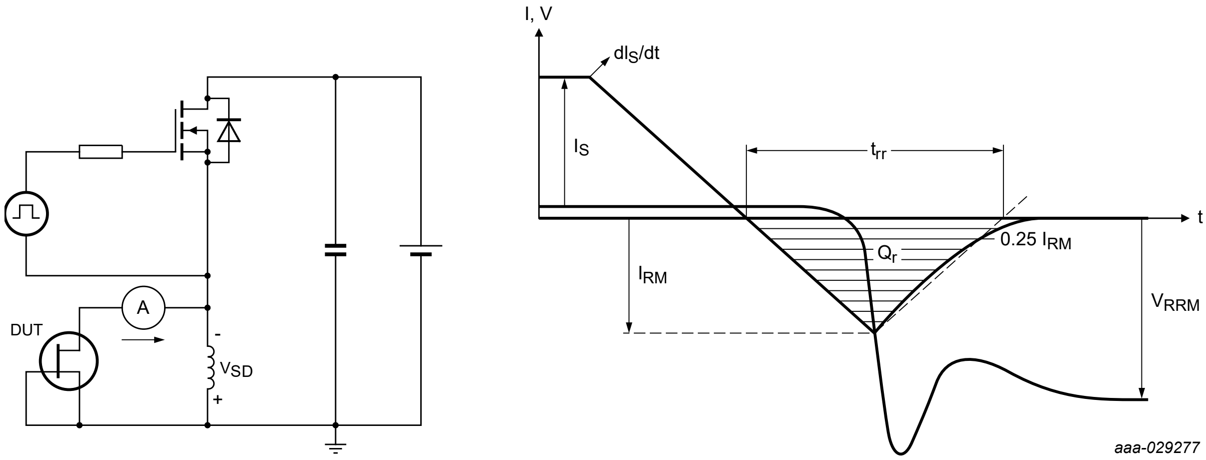


Fig. 3. Diode reverse recovery test circuit and waveform

11. Application information

A Ferrite bead must be fitted in series with the gate of the GaN FET and should be located as close as possible to the gate pin, (see figure below). Keeping the gate-source loop as compact as possible minimizes the gate loop inductance. The Ferrite bead damps the resonant circuit made up of the gate source loop inductance and the GaN FET input capacitance, thus providing fast switching stability. It is recommended that the impedance of the ferrite bead should be 30 Ω @ 100 MHz, (recommended p/n BLM18PG300SN1D). A series resistance (R_G) of 10 - 15 Ω is also recommended.

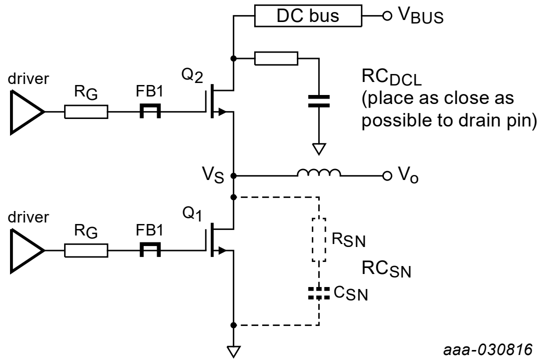
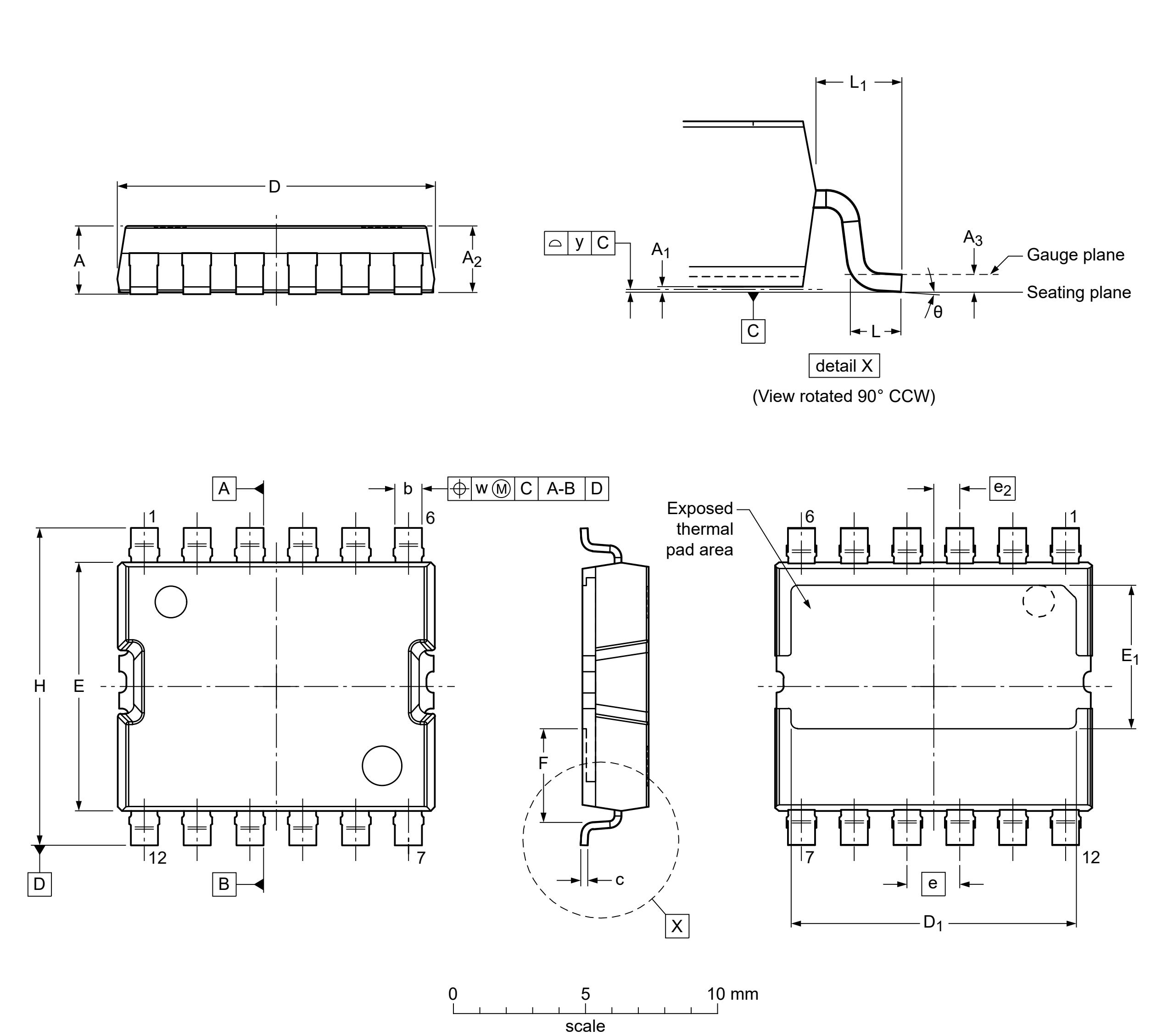


Fig. 4. Ferrite bead and RC snubber

A DC-link snubber is recommended in all cases. Optimal is 20 nF in series with 4 Ω, most easily achieved with parallel combination 10 nF and 8 Ω. This snubber lowers the Q factor of any resonance in the bus. That resonance will act as a load on the high gain amplifier that is the GaN FET and can lead to instability.

12. Package outline

Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body **SOT8000**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b	c	D	D_1	E	E_1	F	e	H	L	L_1	w	y	θ
	max	2.8	0.15	2.65		1.15	0.30	12.2	11.1	9.6	5.7			12.3	1.0				8°
mm	nom				0.25							(3.6)	2.0	12.0		1.3	0.25	0.1	
	min	2.4	0	2.35		0.9	0.24	11.8	10.5	9.2	5.15			11.7	0.6				0°

Note

1. Plastic or metal protrusions of 0.2 mm max per side are not included.

sot8000_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8000						~~20-09-16~~ 20-09-30

Fig. 5. Package outline CCPAK (SOT8000)

13. Soldering

Footprint information for reflow soldering of CCPAK1212 package **SOT8000**

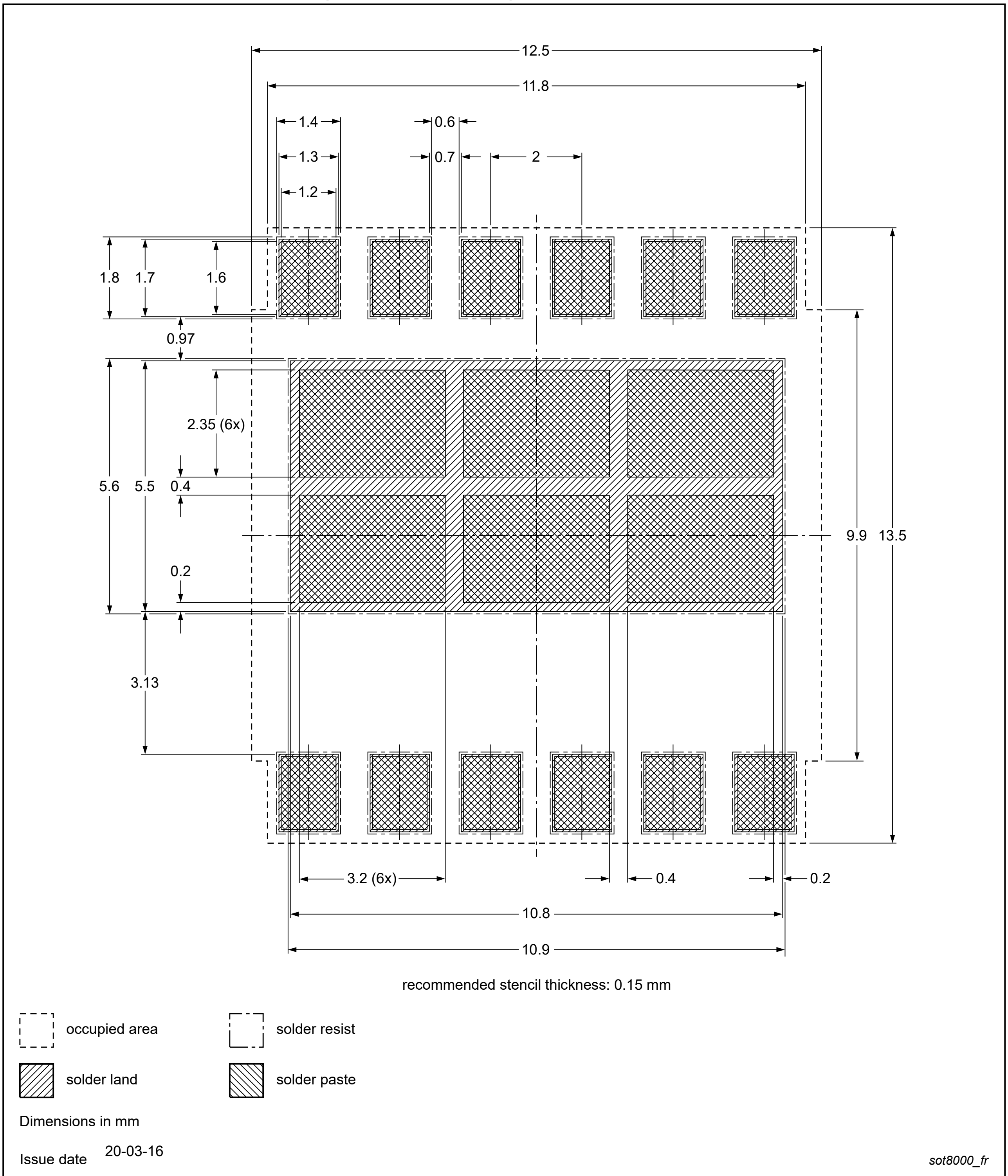


Fig. 6. Reflow soldering footprint for CCPAK (SOT8000)

14. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".
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